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Sarkar et al.

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(54) **JUNCTION-LESS INSULATED GATE
CURRENT LIMITER DEVICE**

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 134 days.

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ABSTRACT

(60) Provisional application No. 61/864,271, filed on Aug.
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on Mar. 6, 2014.

In one general aspect, an apparatus can include a semicon-
ductor substrate, and a trench defined within the semicon-
ductor substrate and having a depth aligned along a vertical
axis, a length aligned along a longitudinal axis, and a width
aligned along a horizontal axis. The apparatus includes a
dielectric disposed within the trench, and an electrode dis-
posed within the dielectric and insulated from the semicon-
ductor substrate by the dielectric. The semiconductor sub-
strate can have a portion aligned vertically and adjacent the
trench, and the portion of the semiconductor substrate can
have a conductivity type that is continuous along an entirety
of the depth of the trench. The apparatus is biased to a
normally-on state.

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